Remarks

Applicant notes that this paper is entered in connection with a petition to revive, and thus presents arguments in response to the previous (Final) Office Action dated October 5, 2009, which address new aspects of the rejections that had not been previously discussed. Applicant believes that the following discussion should assist the Examiner in understanding the lack of correspondence in the cited references and errors in the previous rejection. The following further discusses aspects of the new claims as presented herein.

The final Office Action dated October 5, 2009, listed the following rejections: claims 1-2, 4-8, 10-14, 16-18 and 20 stand rejected under 35 U.S.C. § 102(b) over the Sherwood reference ("Predictor-Directed Stream Buffers"); and claims 3, 9, 15 and 19 stand rejected under 35 U.S.C. § 103(a) over the Sherwood reference in view of Handy (the Cache Memory Book). Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully traverses the § 102(b) and § 103(a) rejections because the cited Sherwood reference, either alone or in combination with the Handy reference lacks correspondence. Specifically, the Office Action failed to establish correspondence to limitations directed to only allowing both accesses and updates to a stride prediction table (SPT) in response to the detection of a cache miss. The Office Action relies upon citation to Sections 4.2 and 4.3 of the Sherwood reference (spanning four columns), but does not recite explicitly where the asserted limitations are disclosed. Applicant has reviewed these cited portions and cannot ascertain any discussion of updating the asserted stride table only in response to a cache miss. The Examiner's Response to Arguments asserts that Section 4.2 (3rd paragraph) of the Sherwood reference discloses indexing (accessing) the stride table on a load-PC (for a missed load), but fails to further identify where updating the stride table only in response to a cache miss is discussed.

In view of this lack of correspondence in the cited portions of the Sherwood reference, Applicant has reviewed other portions of the reference and submits that the Sherwood reference teaches that its SPT is accessed once "each cycle…to make a prediction." Because of its every-cycle occurrence, this SPT access necessarily occurs at times other than in response to a detected cache miss. This is consistent with Applicant's

traversals of record. The Response to Arguments section attempts to discard this teaching by asserting that the relied-upon portions of the Sherwood reference (Figure 2, Section 4.1) is "a related, but different, system."

In reply, Applicant submits that Section 4.1 explicitly recites that "Figure 2 shows the general model of our predictor-directed stream buffer architecture." Moreover, the discussion in Section 4.1 is clearly applicable to the remaining discussion as it explicitly involves using "priority heuristics described in section 4.4." This is further consistent with the discussion in section 4.2 on page 5, which indicates that the stride table includes both a last and current address and that the stride is calculated by "current miss address – last address." This further appears necessary to the Sherwood reference's purpose as directed to using this difference calculation to store "only the cache misses" in the Markov table (the difference is not stored when the "last address" is not a cache miss). Accordingly, this architecture applies to the disclosed stride table. Moreover, as no portion of the cited Sections 4.2 and 4.3 discloses updating a stride table only on a cache miss, and as these cited portions do not contradict the related discussion in Section 4.1 (as applicable to "our" architecture as referred to by the authors), Applicant submits that the record fails to support the Examiner's position. In this regard, Applicant submits that the Sherwood based rejections are improper and requests that they be removed for lack of correspondence.

In view of the above, Applicant submits that the rejection of claim 1 is improper. Applicant further submits that the rejections of the other independent claims 11 and 17 is similarly improper for failing to correspond to similar limitations, as the same portions of the Sherwood reference are generally relied upon. For example, the cited portions of the Sherwood reference fail to disclose "a filter circuit preventing both accesses and updates to the SPT unless a cache miss is detected" as in claim 11, or "restricting accesses to the SPT in response to the detection of a cache miss" as in claim 17.

Applicant further submits that the rejections of the dependent claims are improper for reasons including those stated above in connection with the independent claims from which they depend. However, the Office Action has also failed to establish correspondence to various dependent claim limitations. Regarding claims 6 and 7 by way of example, the Office Action's assertion that the cited portions of the Sherwood

reference that operate in response to a cache miss also (apparently inherently) disclose limitations directed to determining whether a processor-executed instruction is a memory access instruction and is devoid of any support in the cited references. To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991) (emphasis added). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.* at 1269 (quoting *In re Oelrich*, 666 F.2d 578, 581 (1981).

In this instance, the Office Action appears to assert that the cited cache-miss functions are "requiring the first two limitations of [Applicant's] claims." However, nothing in the reference supports this assertion; moreover, such information may simply be provided, or a cache miss can be detected in other manners (*e.g.*, based upon functionality that happens after a cache miss). Accordingly, the Office Action has failed to establish that the missing limitations are necessarily present in the cited reference, and the rejections thus fail.

Regarding the § 103(a) rejections, Applicant submits that the rejection fails to provide any explanation or supporting citation as to how the Sherwood reference would function as modified, or as to any motivation for modifying the Sherwood reference as proposed. While the rejections are believed improper for the reasons stated above in connection with the § 102 rejections, Applicant thus believes that the rejections are further improper for these reasons as well.

Applicant has added new claim 21. Applicant believes that claim 21 is allowable over the cited references for reasons including those discussed above, and further because the cited references fail to disclose, teach or suggest limitations directed to executing instructions to access the SPT and predict a cache miss based upon an update to the SPT indicative of one of said detected cache misses, and controlling the loading of a stream cache based upon the memory location of the load access instruction in response to a predicted cache miss. Support for these limitations can be found throughout the specification and figures, with exemplary embodiments shown in Figures 6a-6b and 7a-

7c, as well as the discussion at paragraphs 0039-0043 of Applicant's published application.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, David Schaeffer, of NXP Corporation at (212) 876-6170.

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